REMARKS

The enclosed is responsive to the Office Action mailed on July 25, 2008. At the time the Examiner mailed the Office Action claims 1-23 were pending. By way of the present response Applicant has amended claim 1 to include the subject matter of claim 22 in order to more particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claim 22 has been canceled. No new claims have been added. As such, claims 1-21 and 23 are now pending. Applicant respectfully requests reconsideration of the present application and the allowance of all claims now presented.

Applicant teaches and claims in claims 1-21 and 23 a method for producing a substrate suitable **for subsequent use in semiconductor processing.** That is, the process taught and claimed by Applicant in claims 1-21 and 23 concerns treating the substrate ***which may then be used*** in the production of semiconductor assemblies. The method includes roughening the surface of the substrate material, treating the roughened surface with a strong acid, and **applying a dielectric coating composition containing at least one metal oxide onto the roughened surface** to provide a non-conductive surface suitable for subsequent use in semiconductor processing.

The roughening is characterized as creating microfissures and may additionally leave microparticles of the substrate material on the roughened surface. The strong acid etch treatment effectively to removes loosely held microparticles of the substrate material on the roughened surface, however, Applicant has observed that **the microfissures of the roughened surface can still form additional particles during the production of semi-conductor assemblies.** For example, jagged edge pieces of the microfissures can be dislodged or broken off from the surface and thus

the microfissures themselves may be a source of undesirable loose particles after the strong acid etch.

Accordingly, Applicant teaches and claims in claims 1-23 to **apply a dielectric coating** composition containing at least one metal oxide onto the roughened surface to prevent the dislodgment of any microparticles of the substrate material that may be present in the microfissures, and additionally prevent jagged edge portions of the microfissures from dislodging to become loose particles. Thus, Applicant teaches and claims in claims 1-21 and 23 a method of treating the surface of a substrate material, which includes sealing a roughened surface with a dielectric coating composition containing a metal oxide, so that small particles are not generated during subsequent use in the production of semiconductor assemblies.

Claim Rejections – 35 U.S.C. § 102

The Examiner rejected claims 1-3, 9-14, 16-19, 22 and 23 under 35 U.S.C. § 102(b) as being anticipated by *Gorczyca et al.* (US Pub 2002/0094686).

It is Applicant's understanding that *Gorczyca* discloses a method of processing a semiconductor article to be subsequently used in a low pressure chemical vapor deposition (LPCVD) furnace for prolonged periods without requiring cleaning to remove the built-up film. (Abstract). The semiconductor processing article is prepared for subsequent use in the LCPVD furnace by mechanically roughening and chemically roughening the quartz surface of the article. (paragraph [0005]). The final surface of the semiconductor processing article prior to providing it to the LPCVD furnace for extended use is an uncoated surface characterized by a surface roughness having a first component due to the mechanical roughening and a second component due to the chemical roughening. Then, as discussed in paragraphs [0003], [0022], [0023], and [0034], a **silicon film** may be deposited onto the surface of the semiconductor article **during extended use**

in an LPCVD furnace. This silicon film may even oxidize and expand to completely fill the trenches.

Applicant respectfully submits that *Gorczyca* fails to disclose or suggest each and every element of the invention as claimed in at least two significant respects. Foremost, *Gorczyca* fails to disclose or suggest the element of "applying a dielectric coating composition ... onto the roughened surface." Secondly, *Gorczyca* fails to disclose or suggest applying a dielectric coating composition "for subsequent use in semiconductor processing" as is taught and claimed by Applicant in independent claim 1.

Firstly, Applicant respectfully submits that *Gorczyca* fails to disclose or suggest the element of "applying a dielectric coating composition ... onto the roughened surface." To the contrary, *Gorczyca* discloses applying a silicon film, which is a semi-conductor and not a dielectric, and then subsequently converting a portion of the silicon film into silicon oxide. In no part does *Gorczyca* disclose applying a silicon oxide film onto the roughened surface. Accordingly, *Gorczyca* does not disclose applying a dielectric coating composition onto the roughened surface, as is taught and claimed by Applicant in independent claim 1.

Secondly, Applicant respectfully submits that *Gorczyca* fails to disclose applying a dielectric coating composition for subsequent use in semiconductor processing. It is Applicant's understanding that *Gorczyca* does not apply a film (such as the silicon film) on the semiconductor article until after providing the providing the semiconductor article to a LPCVD apparatus for extended use. The "Background of the Invention" section puts into context the disclosure of document *Gorczyca*. When a semiconductor article is used in a LPCVD furnace, films are deposited on the semiconductor article that are as thick as the layers that are

deposited on the substrate. The film build-up causes a stress from the coefficient of thermal expansion (CTE) difference between **silicon** (2.9 ppm/°C) or silicon nitride (5.0 pm/°C) and **quartz semiconductor article** (0.5 ppm/°C). Eventually, after extended use this stress induces cracking in the surface of the quartz semiconductor article.

As discussed in paragraphs [0003], [0022], [0023], and [0034], a **silicon film** may be deposited onto the surface of the semiconductor article **during extended use** in an LPCVD furnace. This silicon film may even oxidize and expand to completely fill the trenches. To the contrary, Applicant teaches and claims in claims 1-21 and 23 applying a dielectric coating composition onto the roughened surface for subsequent use in semiconductor processing.

Therefore, Applicant respectfully submits that the invention claimed in claims 1-3, 9-14, 16-19 and 23 is not anticipated by *Gorczyca* under 35 U.S.C. § 102(a) and respectfully requests the withdrawal of the rejections of the claims.

Claim Rejections – 35 U.S.C. § 103

Claims 4 and 15

The Examiner has rejected claims 4 and 15 under 35 U.S.C. § 103(a) as being unpatentable over *Gorczyca et al.* (US Pub 2002/0094686) as applied to claim 3, in view of *Choi* (US Patent 6,833,279). In particular the Examiner states "Specifically, Choi teaches yttrium oxide layer (i.e. a dielectric coating) deposited on a roughened ceramic surface." Applicant disagrees.

As described above, it is Applicant's understanding that *Gorczyca* discloses a method for preparing an article for subsequent use in an LPCVD **deposition furnace**, which includes roughening a surface. Once in the LPCVD deposition

chamber, process films such as Si adhere to the roughened surface of the article and do not flake off.

It is Applicant's understanding that *Choi* discloses a method for preparing a component for subsequent use in a plasma **etch chamber**. A dielectric layer (i.e. yttrium oxide) is applied a component using a plasma spray. The dielectric layer has excellent plasma and chemical resistance to etch processes. Col. 2, ll. 45. During use in a plasma etch chamber the dielectric layer itself is etched and becomes rugged (step S400 of FIG. 2). Therefore, the dielectric layer can then be subsequently removed (step S500 of FIG. 2) and reapplied (step S600 of FIG. 2). **At no point does *Choi* disclose or suggest depositing the dielectric coating on a roughened surface including microfissures.**

As neither *Gorczyca* nor *Choi* disclose applying a dielectric coating onto a roughened surface including microfissures, as is claimed by Applicant in independent claim 1, the combination cannot be interpreted to disclose the claimed element.

Furthermore, Applicant respectfully asserts that one of ordinary skill in the art would not be motivated to add the chemically resistant dielectric coating of *Choi* to the article of *Gorczyca*. As a practical matter, there would be no practical benefit of implementing a chemically resistant dielectric coating to the article of *Gorczyca*. As described above, the chemically resistant dielectric coating of *Choi* is for application in a plasma etch chamber, while the article of *Gorczyca* is for application in an LPCVD chamber. Accordingly, Applicant submits that one of ordinary skill in the art would not be motivated to make the proposed modification.

Therefore, the combination cannot render obvious Applicant's invention as claimed in claims 4 and 15, and Applicant respectfully requests the withdrawal of the rejection of the claims under 35 U.S.C. § 103(a) over the combination.

Claims 5-8, 20 and 21

The Examiner has rejected claims 5-8, 20 and 21 under 35 U.S.C. § 103(a) as being unpatentable over *Gorczyca et al.* (US Pub 2002/0094686) in view of *Kowalsky et al.* (US Patent 6,861,101) and in further view of *Choi* (US Patent 6,833,279).

It is Applicant's understanding that *Kowalsky* discloses a method of operating a plasma torch. However, at no point does *Kowalsky* disclose or suggest depositing the dielectric coating on a roughened surface including microfissures as is taught and claimed by Applicant in independent claim 1.

Therefore, in view of the above comments regarding *Gorczyca* and *Choi* the combination cannot render obvious Applicant's invention as claimed in claims 5-8, 20 and 21, and Applicant respectfully requests the withdrawal of the rejection of the claims under 35 U.S.C. § 103(a) over the combination.

Pursuant to 37 C.F.R. § 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. §§ 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

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